REMARKS

In the Office Action dated March 11, 2004, the Examiner rejected claims 1-2, 5-7, 10-12 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Vaidyanathan et al. (U.S. Patent No. 6,053,948) in view of Sakamoto (U.S. Patent No. 4,617,660); and rejected claims 3-4, 8-9, and 13-14 under 35 U.S.C. § 103(a) as being unpatentable over Vaidyanathan et al. in view of Sakamoto, and further in view of Takamisawa et al. (U.S. Patent No. 5,337,317). The Examiner also objected to the Specification on the basis that different terms were used to designate the same test address information in both the Specification and the Drawings. The Examiner objected to the Drawings due to a misspelled term and a control signal that was drawn as bi-directional instead of unidirectional.

By this Amendment, Applicants cancel, without prejudice or disclaimer of the subject matter thereof, claims 1-15. In addition, Applicants amend the Specification and the Drawings. Finally, Applicants add claims 16-27. In view of the following remarks, Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103(a) and objections to the specification and drawings.

The Examiner objected to the term in the Specification, "TEST_ADDR," as used on page 11, lines 7, 9, and 12, in view of Fig. 2, which was labeled with the term "TEST_ADDRESS." In response, Applicants have replaced the term "TEST_ADDRESS" with the term "TEST_ADDR" in Fig. 2 to conform with the terms on page 11, lines 7, 9, and 12.

The Examiner objected to a misspelled term in the Drawings. In response, Applicants have replaced the misspelled term, "TEST_MODO," in Fig. 2 with the correctly spelled term, "TEST_MODE."

Further, the Examiner objected to the "CONTROL" signal in the Drawings that was drawn as bi-directional instead of unidirectional. In response, Applicants have replaced the bi-directional signal with a unidirectional "CONTROL" signal in Fig. 1 between test master model 11 and LSI model 12.

The Examiner rejected claims 1-2, 5-7, 10-12, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Vaidyanathan et al. in view of Sakamoto.

Present claim 16, which has replaced canceled claim 1, recites "[a] method of simulating an operation of memory, comprising: supplying a memory address, which includes a first bit set for specifying a location to be accessed in a memory model and a second bit set for specifying an error address on which an error is to be generated, to the memory model describing the operation of the memory, thereby to simulate a read/write operation corresponding to the location specified by the first bit set of the memory address; and generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set."

Applicants respectfully submit that Vaidyanathan et al. in view of Sakamoto does not disclose this claimed combination of steps. Among other things, the references do not disclose at least a method of simulating an operation in memory "generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set[]" as recited in claim 16.

Vaidyanathan et al. discloses a system including a memory model of a memory circuit containing a number of address bits, a number of data bits, and a memory type parameter. See Abstract. When one embodiment of the memory model is used for simulation, a memory model tree is generated "that tracks the data written to the memory model." See col. 3, lines 18-23. Further, the memory model may include a transaction log which "allows the designer to roll a simulation back. . . . reveal[ing] an error in the operation of the circuit model" enabling the designer "to better understand the error." See col. 16, lines 41-47.

In contrast, methods and systems consistent with the present claimed invention can force an error at a designated location in the memory model, as recited in claim 16. Forcing an error at a specific memory location is a different concept than rolling back a simulation to better understand an existing error as disclosed Vaidyanathan et al. The concept of placing the error in memory is not taught or suggested by Vaidyanathan et al. Moreover, the Examiner admits that Vaidyanathan et al. reference "does not expressly disclose generating an error." See Office Action, page 4. Therefore, Vaidyanathan et al. does not teach, disclose or suggest "generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set[]" as recited in claim 16.

Sakamoto fails to overcome the aforementioned deficiencies of Vaidyanathan et al. Sakamoto discloses "a faulty-memory processing method and apparatus having an ECC [Error Correction Code] error detection and correction function" to minimize the

effect on "processing capability due to correction of a hard error." See col. 2, lines 6-11. Sakamoto uses error correction means to detect a hard error and to transcribe the corrected information into "relief memory" where the data can be stored until the hard error is corrected later. See col. 2, lines 14-22. Further, Sakamoto performs this transcription during breaks in a time-sharing data process to minimize the decrease in processing capability. See col. 2, lines 23-25.

In contrast, methods and systems consistent with the present claimed invention can force an error at a designated location. Forcing an error to be generated at a specific memory location is different than recording the location of an memory error after it is discovered as disclosed by Sakamoto. The concept of forcing an error in memory is not taught or suggested by Sakamoto. Therefore, Sakamoto does not teach, disclose or suggest "generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set[]" as recited in claim 16.

Accordingly, Sakamoto, either alone or in combination with Vaidyanathan et al., does not disclose, teach, or suggest at least a method of simulating an operation in memory "generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set[]" as recited in claim 16.

The Examiner has provided ambiguous reasoning as to the motivation to combine the Vaidyanathan et al. and Sakamoto references. The Examiner contends that "one of ordinary skill in the art would have been motivated to illustrate a particular memory model that can be used in electronic design automation systems to allow designers to simulate the operation of memory circuits with different stimuli using descriptions of memory circuits," but the Examiner does not provide a clear reason why such a person of ordinary skill in the art would be motivated in this manner. Accordingly, Applicants submit that the Examiner has not provided proper motivation to combine the references. Moreover, even if the references are properly combinable, as stated above, the combination of the two references would not disclose, teach, or suggest the "generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set[]" as recited in claim 16.

For at least the foregoing reasons, Applicants submit that claim 16 is patentable over Vaidyanathan et al. in view of Sakamoto. Because claims 20 and 24 are independent claims with recitations similar to those in claim 16, Applicants further submit that claims 20 and 24 are patentable over Vaidyanathan et al. in view of Sakamoto for at least the reasons given with respect to claim 16.

Applicants also submit that the teachings of Takamisawa et al. are insufficient to remedy the deficiencies of Vaidyanathan et al. and Sakamoto. Accordingly, no combination of Vaidyanathan et al., Sakamoto, and Takamisawa et al. teaches or suggests the element of claims 16, 20, or 24. Therefore, the Applicants believe claims

16, 20, and 24, are patentable over Vaidyanathan et al. in view of Sakamoto and further in view of Takamisawa et al.

The dependent claims 17-19, 21-23, and 25-27 are allowable not only for the reasons stated above with regard to their respective allowable base claims, but also in light of their own additional features that distinguish them from Vaidyanathan et al. in view of Sakamoto.

Since each of the claims is allowable, Applicants respectfully request the timely allowance of this application.

If an extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Amendment, such extension is requested. If there are any other fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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By: _____
Walter Davis, Jr.
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Attachments: **Replacement Sheets (Figs. 1 and 2)**